# ATLAS Tile Calorimeter Upgrade Program

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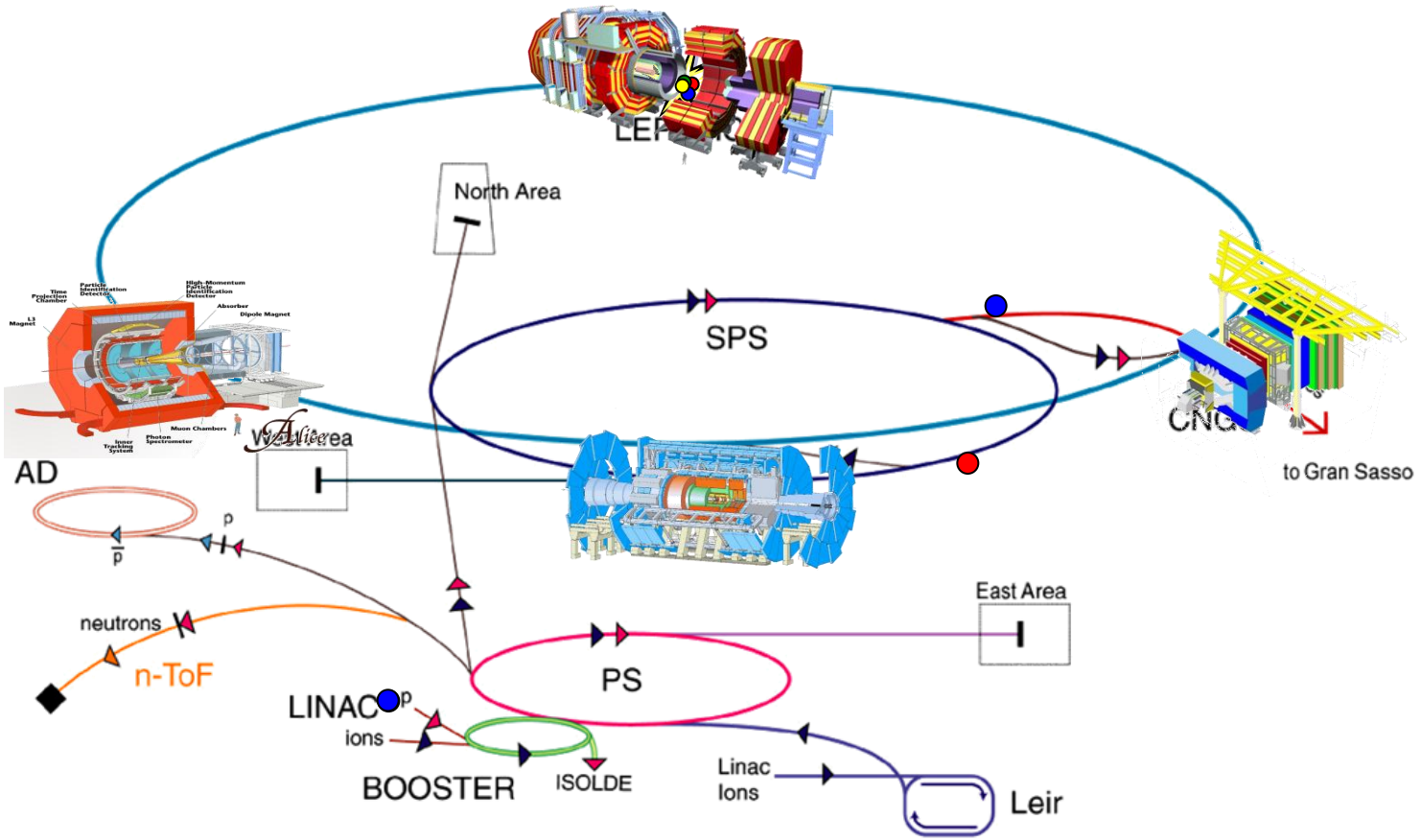
On behalf of TileCal group


Large Hadron Collider
Lake of Gene
CMS
LHCb
ALICE
ATLAS

# Large Hadron Collider

Collision of proton beams… …observed in giant detectors

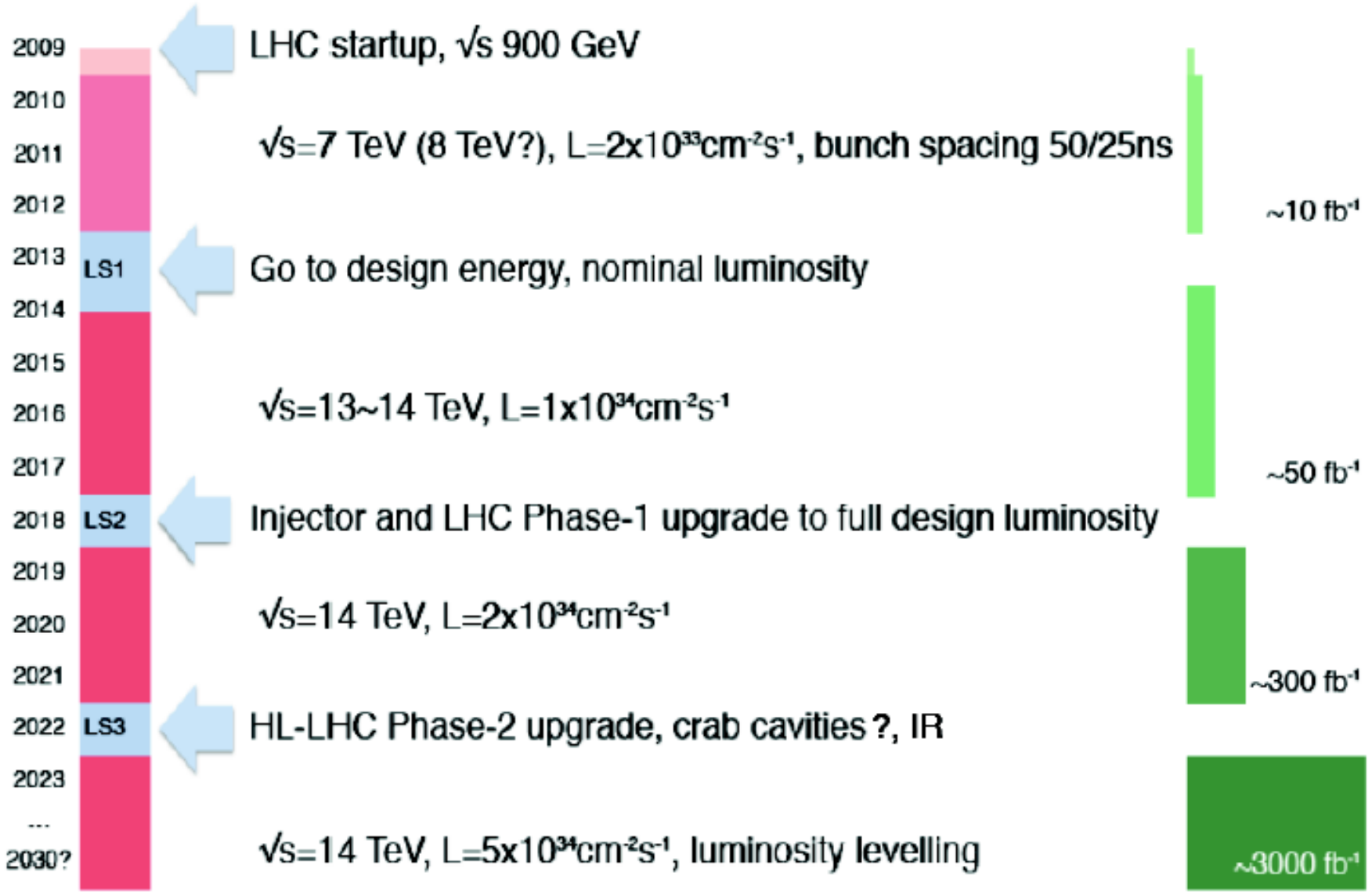



p (proton)
ion
neutron
p̄ (antiproton)
proton/antiproton conversion
neutrino

AD Antiproton Decelerator
PS Proton Synchrotron
SPS Super Proton Synchrotron

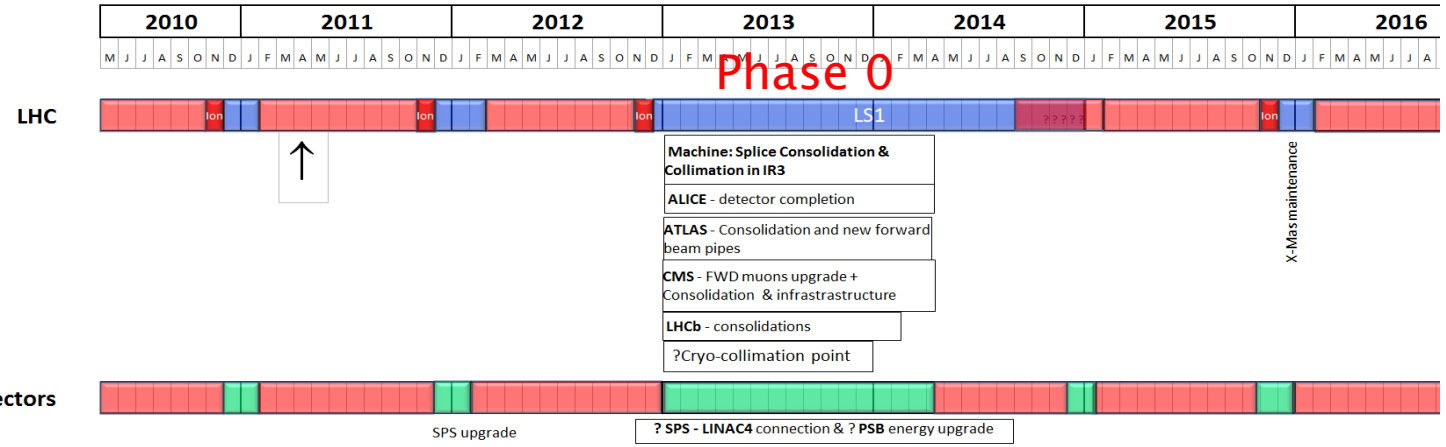
LHC Large Hadron Collider
n-ToF Neutron Time of Flight
CNGS Cern Neutrinos Gran Sasso

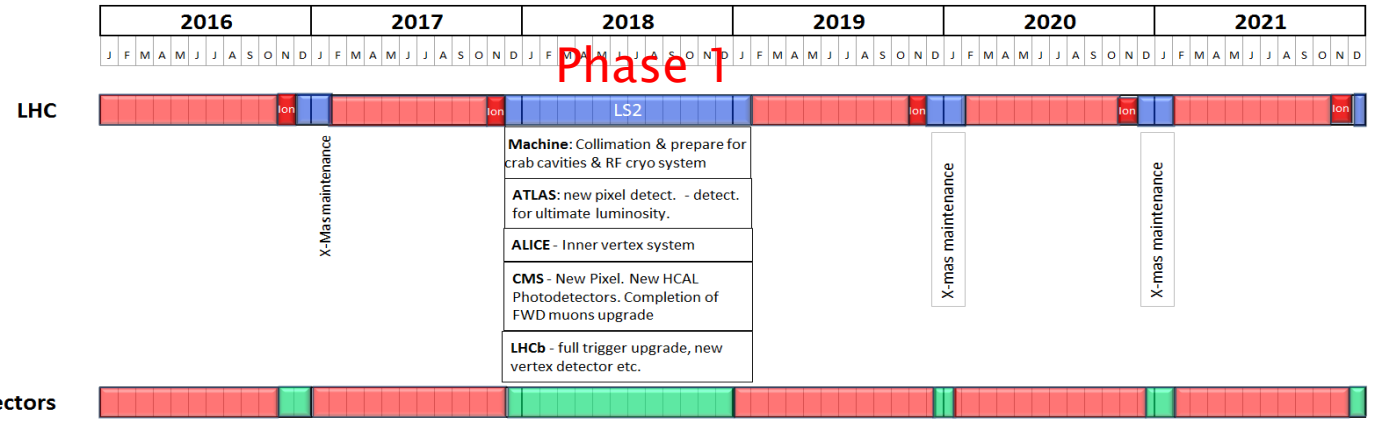
# LHC – evolution plan (preliminary)



# Current (not yet approved) upgrade schedule

New rough draft 10 year plan




Phase 2

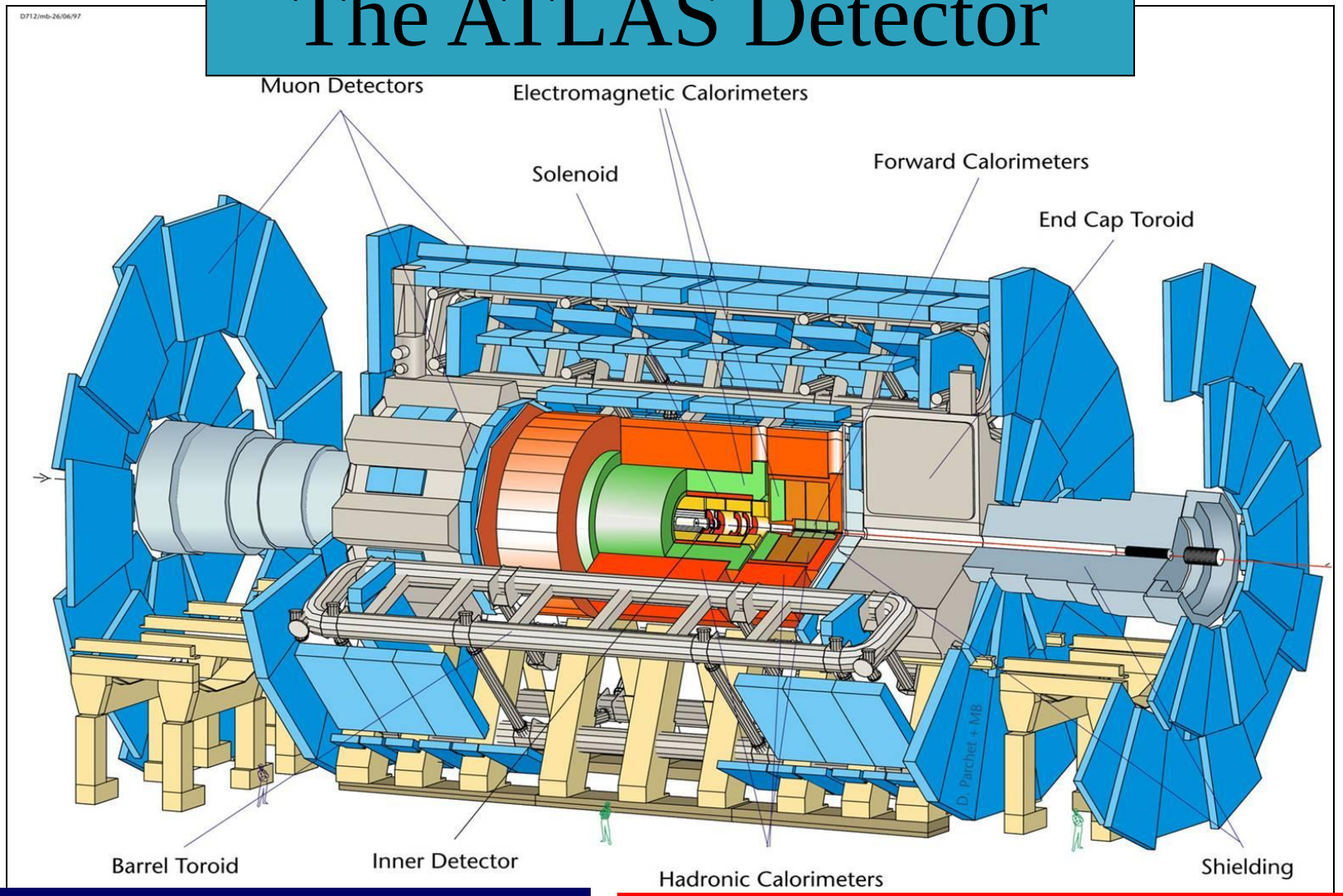
LS3

Installation of sLHC hardware

# Motivation for Upgrade

- Adapt to improved LHC luminosity – factor 10 possible
- Adapt to changing physics requirements
- Remember that much components of detectors must be replaced anyway due to old age and radiation damage

# The ATLAS Detector




| | |
|---|---|
| Diameter | 25 m |
| Total length | 46 m |
| Overall weight | 7000 tons |

Over 2000 scientists and engineers
Nearly 40 countries
More components than a moon rocket

# The present TileCal system

A TileCal drawer contains up to 48 PMT
- Their signals are digitized and stored in a pipeline
- The signals are also combined into tower sums for transfer off the detector via analog trigger cables
- L1a selects sampled pulses for readout to off-detector RODs -1 fiber/drawer

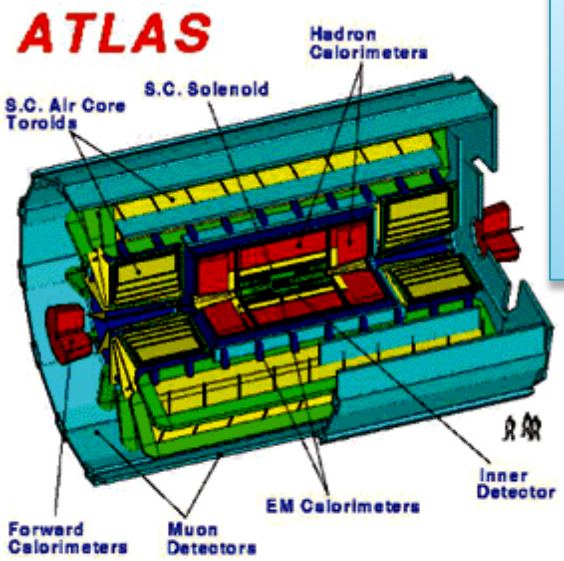
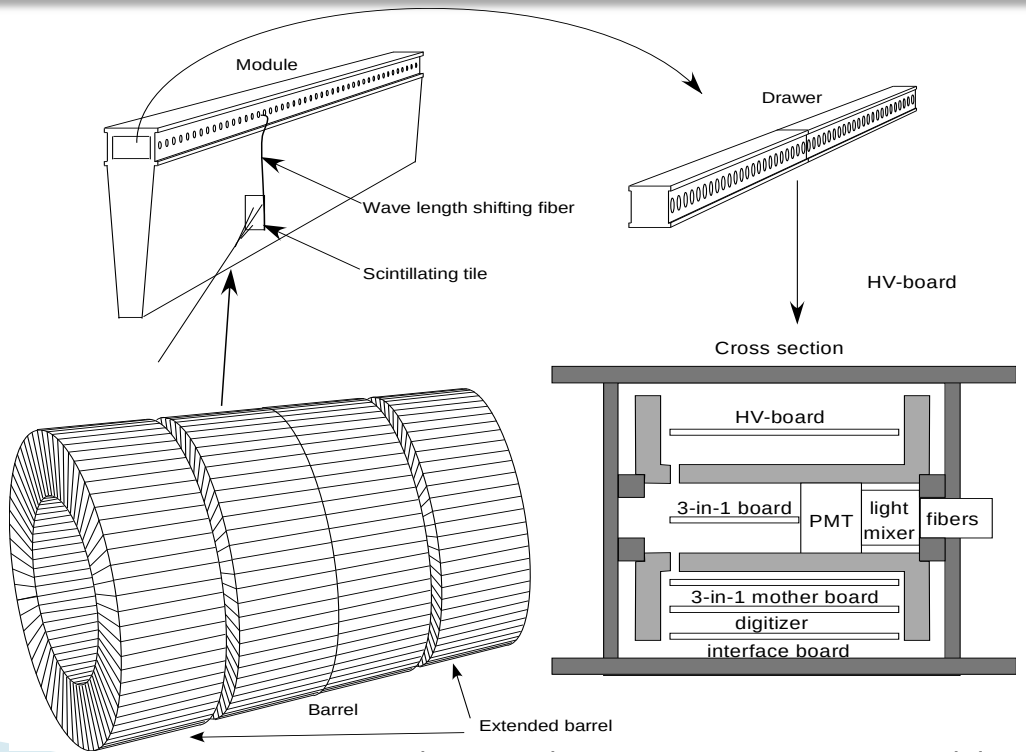
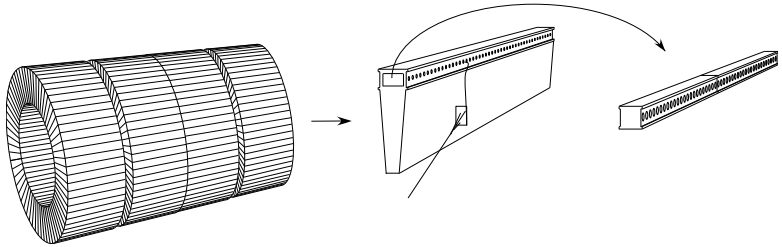
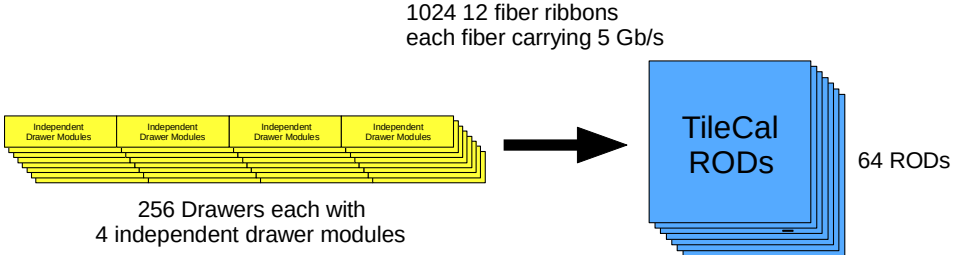



Figure 1: The ATLAS detector.

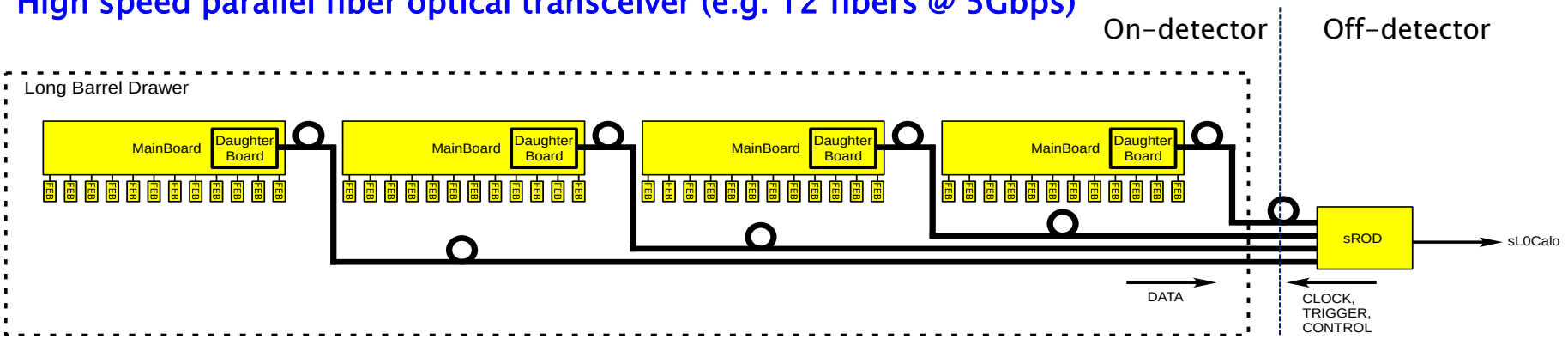


# TileCal Phase 2 Upgrade






- Data bandwidth of entire TileCal with 1024 independent drawer modules -->
  50Tbps with duplication for redundancy
- High speed parallel fiber optical transceiver (e.g. 12 fibers @ 5Gbps)

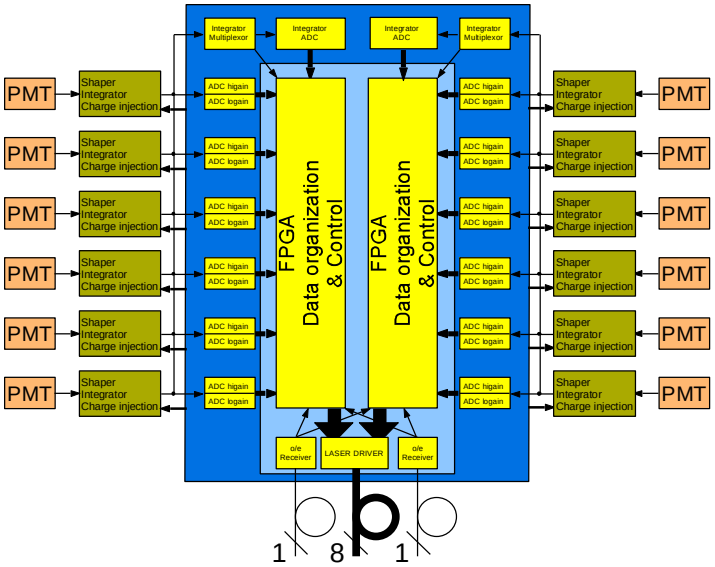



The main components of an upgraded drawer are:

- New front-End boards – three alternative designs (3-in-1, FE-ASIC, QIE)
- MainBoards – digitizing the FE signals
- Processing Daughter Board – processing and high speed communication
- New PMT dividers – new HVPS – new LVPS
- Off detector - sROD modules

# TileCal Phase 2 Upgrade

## Drawer Readout



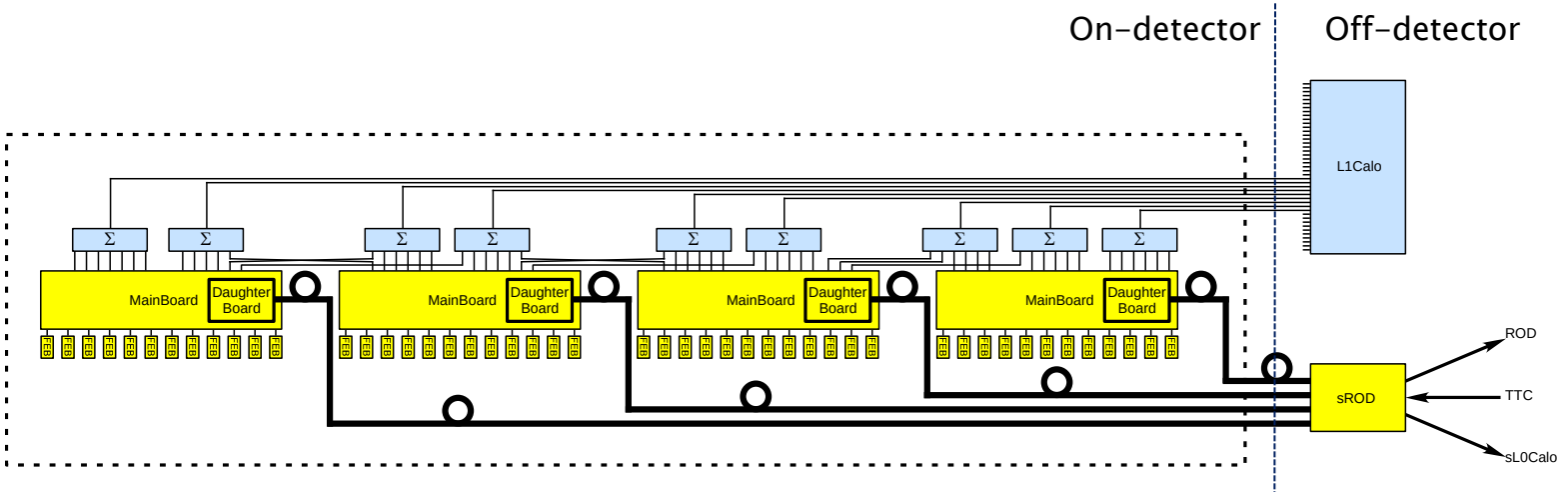

- 4-fold redundancy – all fibers duplicated and 2 channels (on different fibers) per cell
- Clock, Trigger and Control are obtained via the GBT protocol
- Early prototypes are being developed (FE-board agnostic)

# The Calorimeter Readout Demonstrator Project

The Demonstrator project aims at a coordinated yet independent installation of digital trigger data links in a limited area of both LAr and TileCal during LS1 (during 2012-2014).

The new data path should operate in parallel with analog trigger data path thus be compatible with the present trigger and readout

# A TileCal hybrid drawer design

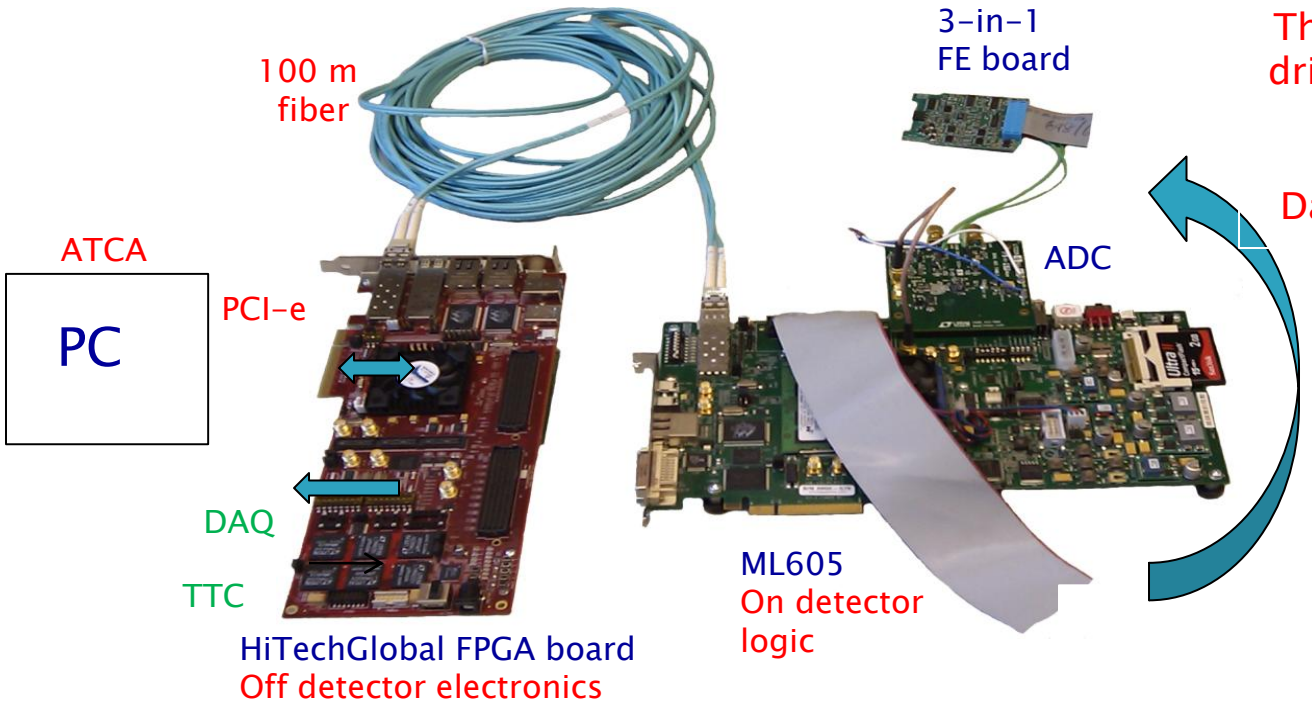



The plan is to develop a hybrid demonstrator drawer compatible with the present system aiming at evaluation in TileCal test facilities before the end of 2013 and then insertion of one hybrid drawer in ATLAS in the end of LS1

Providing analog readout via present summation boards

Firmware in the sROD module interfaces the TTC inputs and the ROD outputs

# A hybrid system test design




A system slice model was assembled for developing firmware for the TileCal upgrade using a combination of dedicated hardware and of the shelf FPGA modules.

This allows developing firmware and also software in parallel with the hardware instead of doing it after the hardware development is finished.

The aim is to gradually replace the model parts with prototype solutions and later with production parts while adapting the firmware successively to the updated hardware.

This will also help to provide test procedures for the evolving system

# Summary

- Maijor upgrade activities for TileCal are planned by phase2 for:

  FE electronics

  ROD system

  High and Low Voltage power suplies

  and before

- TileCal demontrator craition during phase0+phase1
- Development of the firware for TileCal upgrade